Taming release-acquire consistency

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POPL 2016

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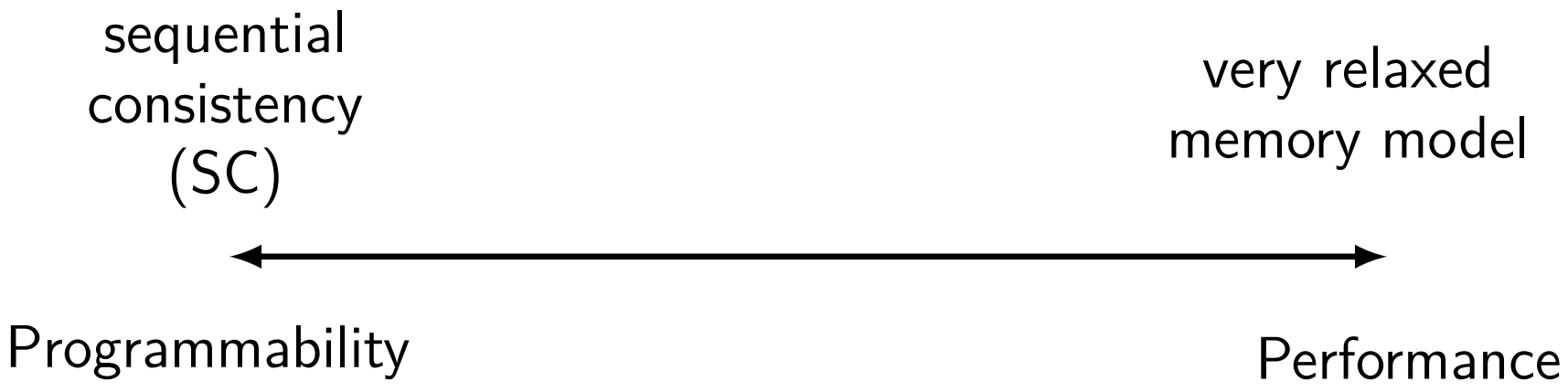

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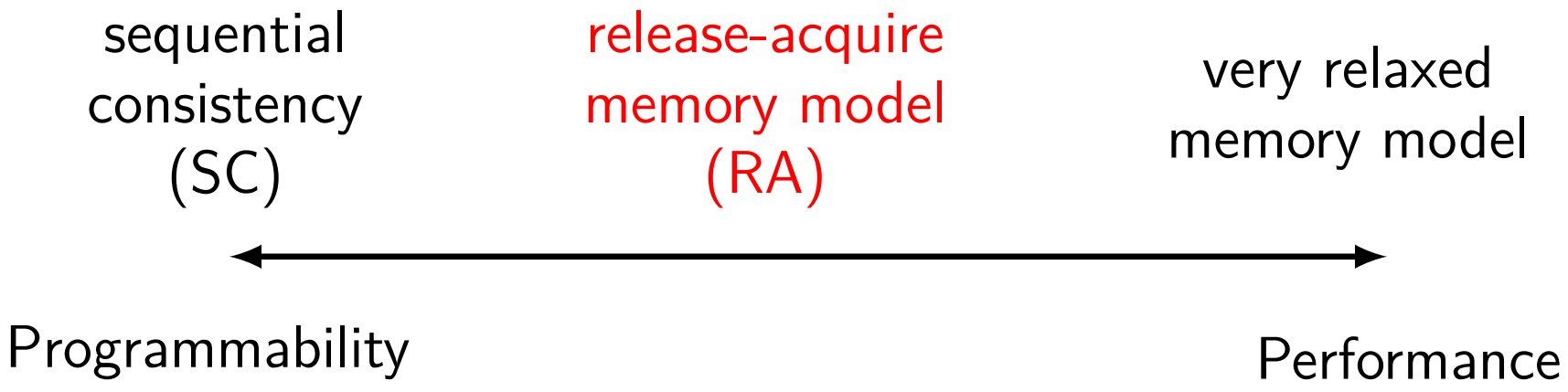

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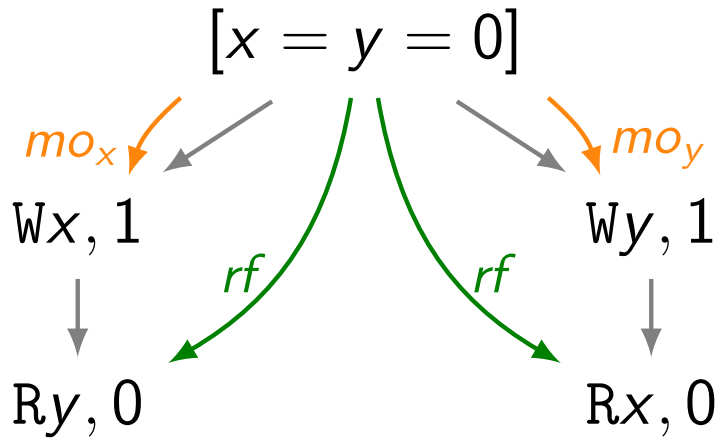

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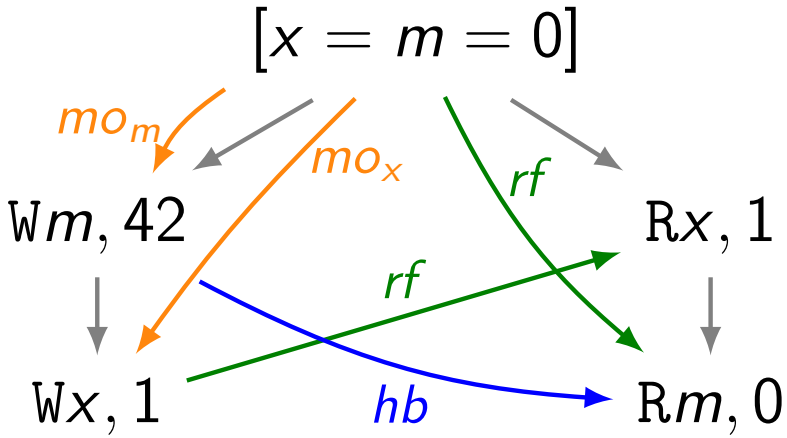


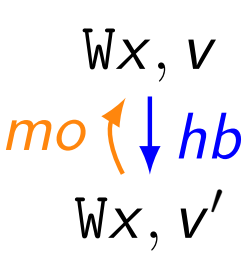
Formal definition

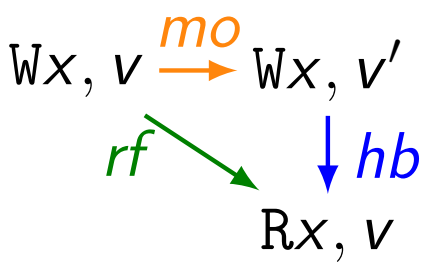
An execution is *consistent* if there are relations:

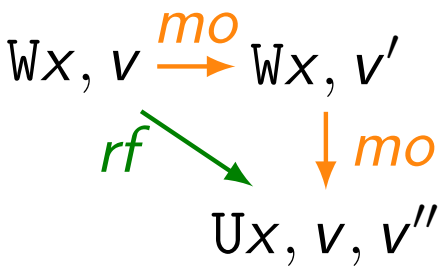
- *reads-from* (*rf*): maps every read to a corresponding write, such that:

  happens-before $= (\textit{program-order} \cup \textit{reads-from})^+$ is irreflexive.

- *modification-order* (*mo*): total order on same-location writes, such that **none of the following occur:**







Good news

- Verified compilation schemes:
  - x86-TSO (trivial compilation) [Batty el al. '11]
  - Power [Batty el al. '12] [Sarkar el al. '12]
- RA supports intended optimizations:
  - In particular, write-read reordering (unlike SC):

$$\mathtt{W}x \rightarrow \mathtt{R}y \quad \rightsquigarrow \quad \mathtt{R}y \rightarrow \mathtt{W}x$$

- DRF theorem (unlike full C11):
  - No data races under SC ensures no weak behaviors
- Monotonicity (unlike full C11, and x86-TSO):
  - Adding synchronization does not introduce new behaviors
- Program logics:
  - RSL [Vafeiadis and Narayan '13]
  - GPS [Turon et al. '14]
  - OGRA [L and Vafeiadis '15]

Bad news

1. Allowed dubious behaviors

2. Overly weak SC-fences

3. No intuitive operational semantics

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Unobservable behaviors

$$x = y = a = b = 0$$

$$\begin{array}{l} x := 1; \\ y := 2; \\ a := 1 \end{array} \;\Big\|\; \begin{array}{l} \texttt{print}\ a; \\ \texttt{print}\ b; \\ \texttt{print}\ x; \\ \texttt{print}\ y \end{array} \;\Big\|\; \begin{array}{l} y := 1; \\ x := 2; \\ b := 1 \end{array}$$

Can this program print $1, 1, 1, 1$?

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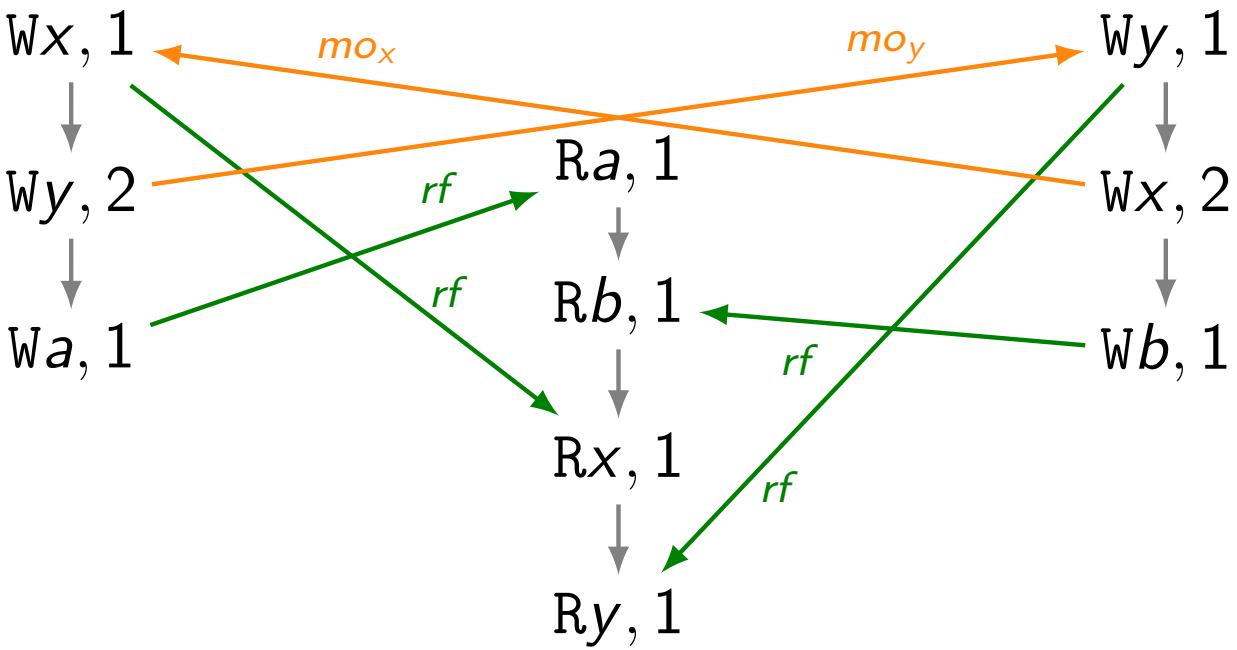

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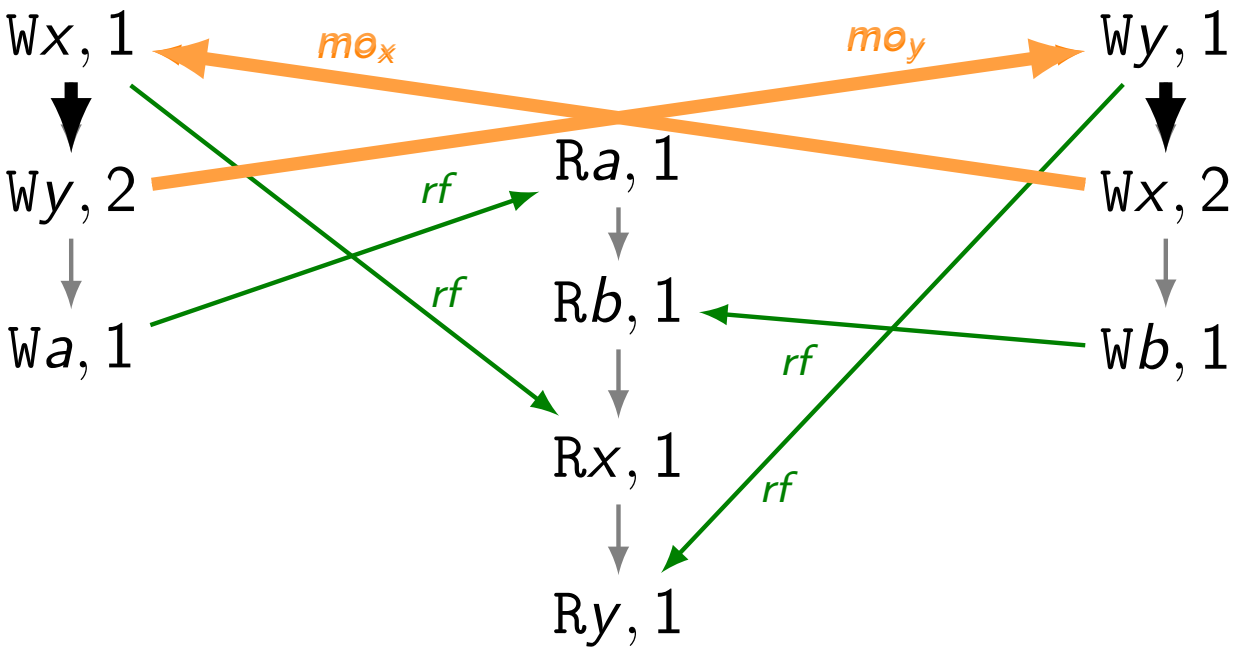

Strong release/acquire consistency

Definition (SRA-consistency)

An execution is *SRA-consistent* if it is RA-consistent and $hb \cup \bigcup_x mo_x$ is acyclic.

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If there are no write-write races then SRA and RA coincide.

Better product, same price

- Same compiler optimizations are sound.
- Compilation to x86-TSO and Power is still correct.

* *No better deal* for Power:

Power model restricted to RA accesses = SRA

(based on Power's declarative model of [Alglave et al. '14])

2. Using Fences to Recover SC

C11's SC-fences

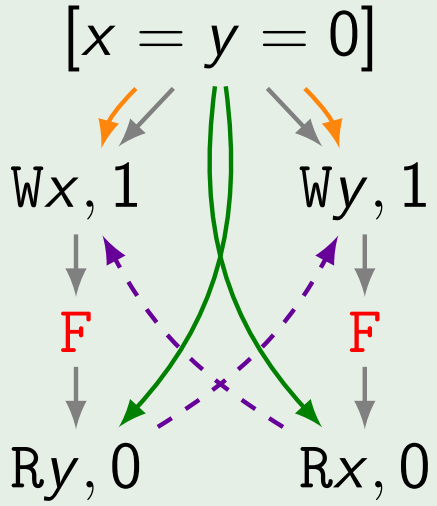
- The strongest fence instruction provided by C11 is *SC*-fence.

Example (Store Buffering)

$$x = y = 0$$

$x := 1;$	$\parallel$	$y := 1;$
`fence();`	$\parallel$	`fence();`
`print` y	$\parallel$	`print` x

printing 0 in both threads is disallowed



Inconsistent: $(\mathtt{F} \times \mathtt{F}) \cap (po^?; (hb \cup mo \cup fr); po^?)$ is cyclic.

- Using the semantics of [Batty et al. '16].

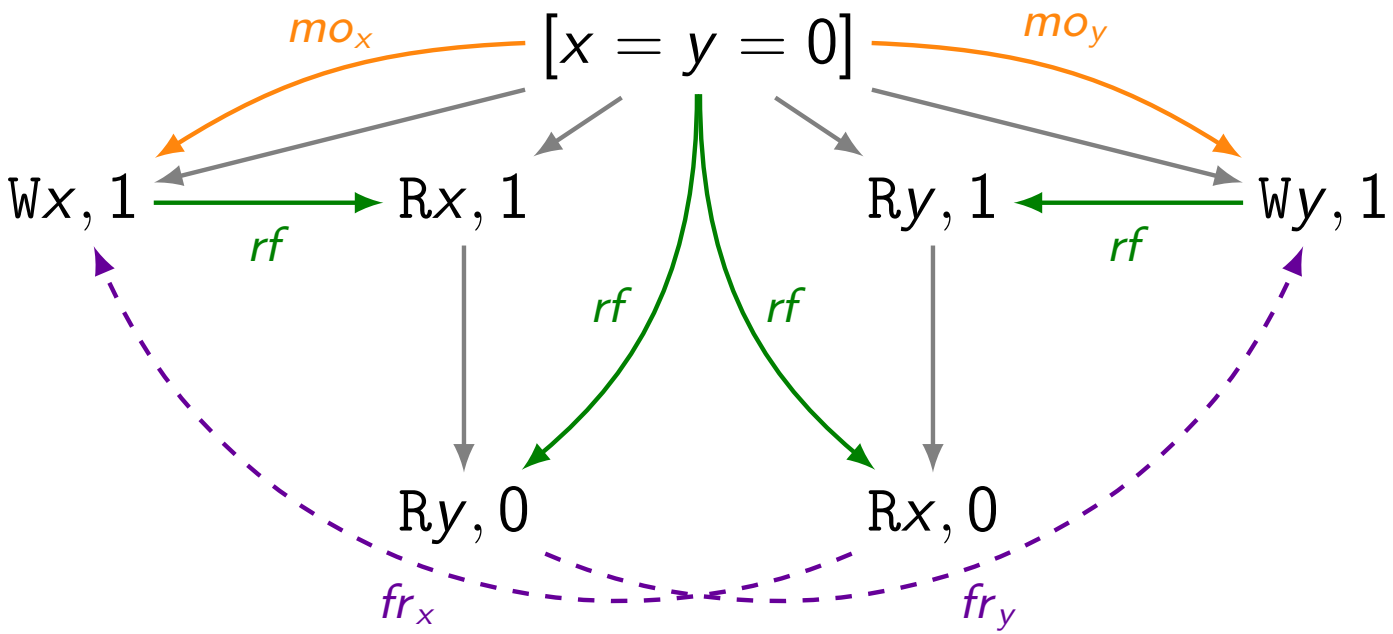
SC-fences are overly weak

Independent reads, independent writes

$$x = y = 0$$

$$x := 1 \;\Big\|\; \begin{array}{l}\texttt{print } x;\\ \\ \texttt{print } y\end{array} \;\Big\|\; \begin{array}{l}\texttt{print } y;\\ \\ \texttt{print } x\end{array} \;\Big\|\; y := 1$$

both threads may print $1, 0$



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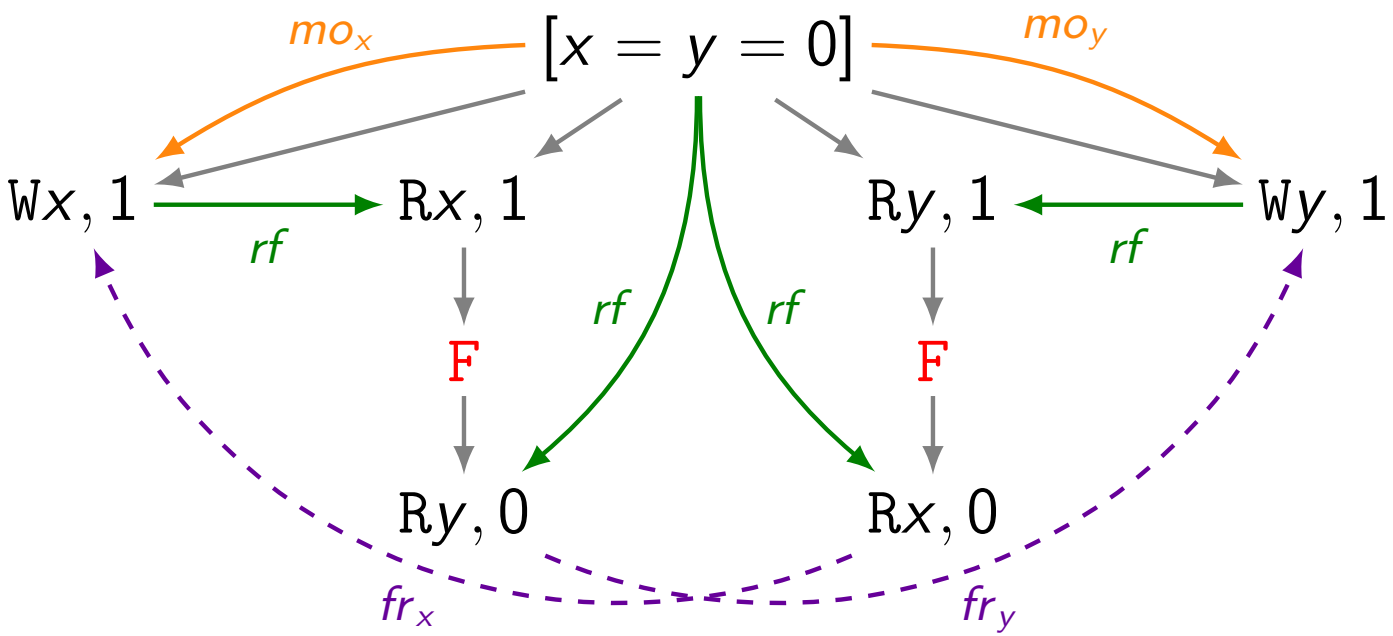

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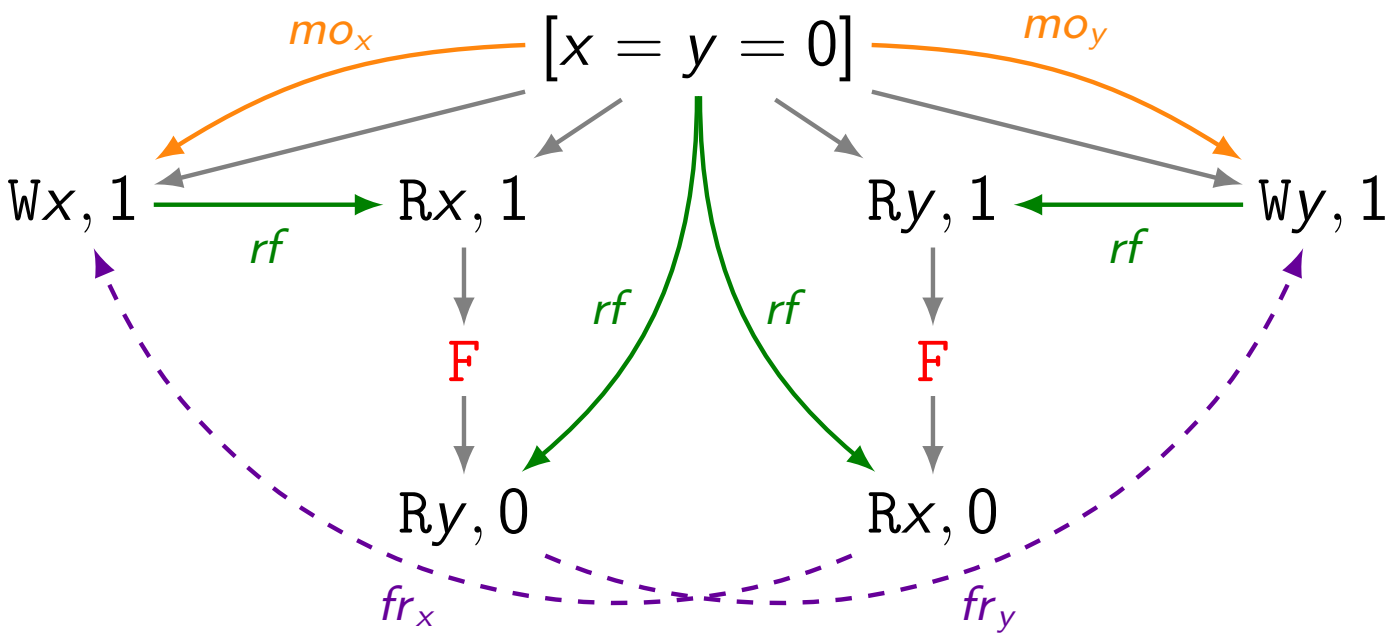
Our suggestion

- Model SC-fences as acquire/release atomic updates of a distinguished fence location.
- RA semantics enforces all fence events to be ordered by *hb*.



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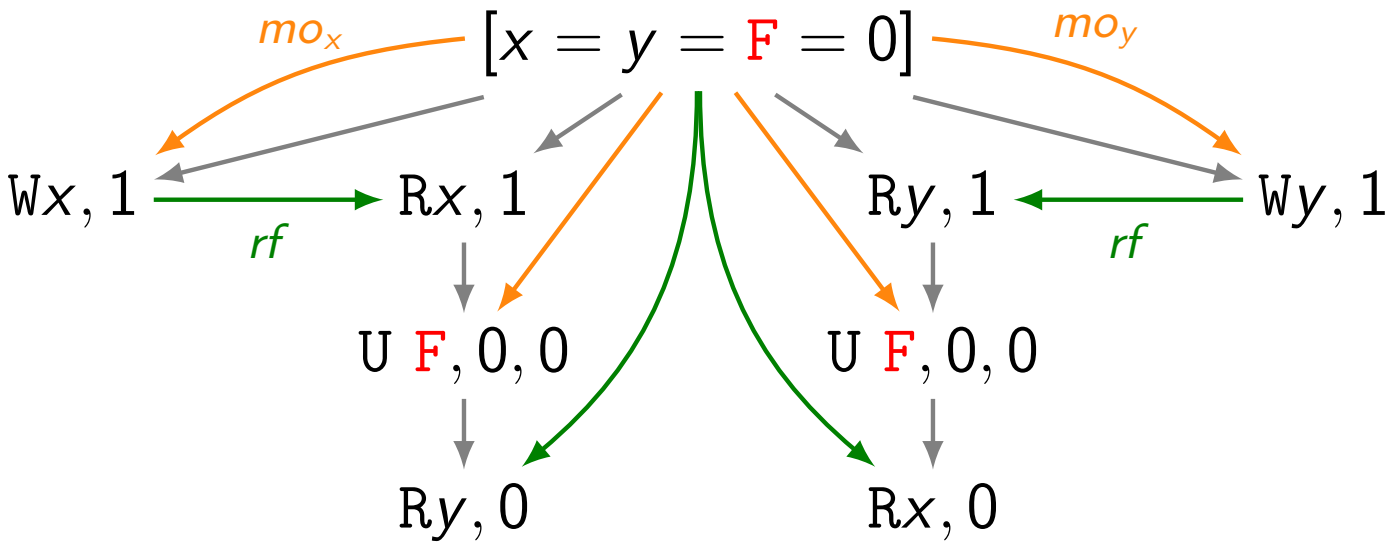

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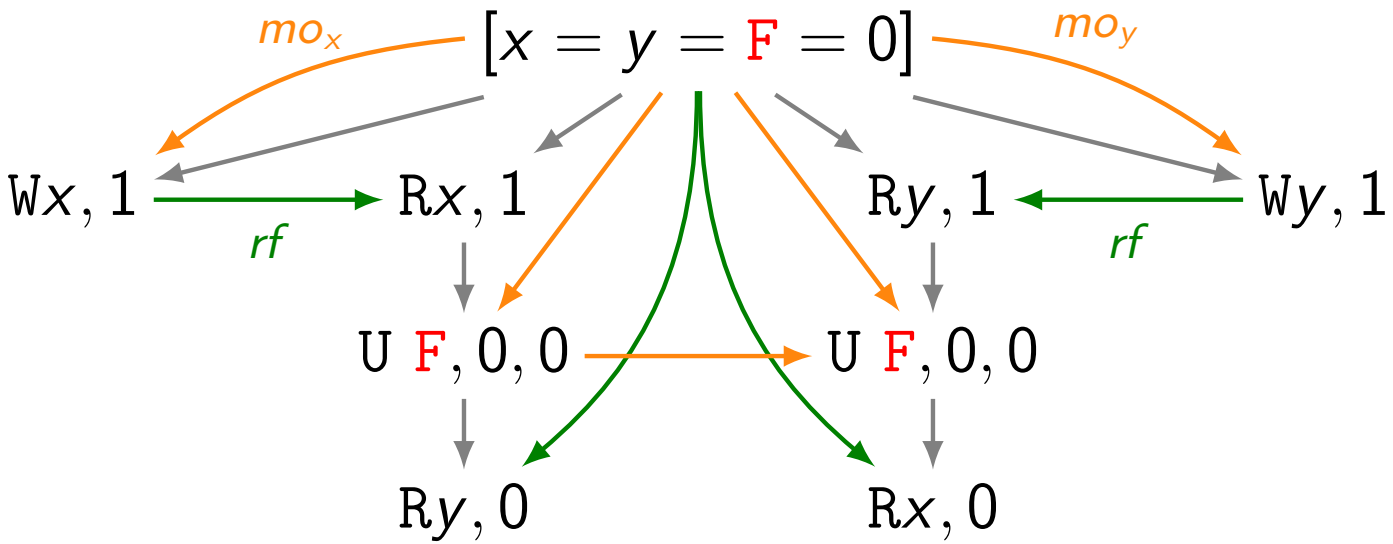

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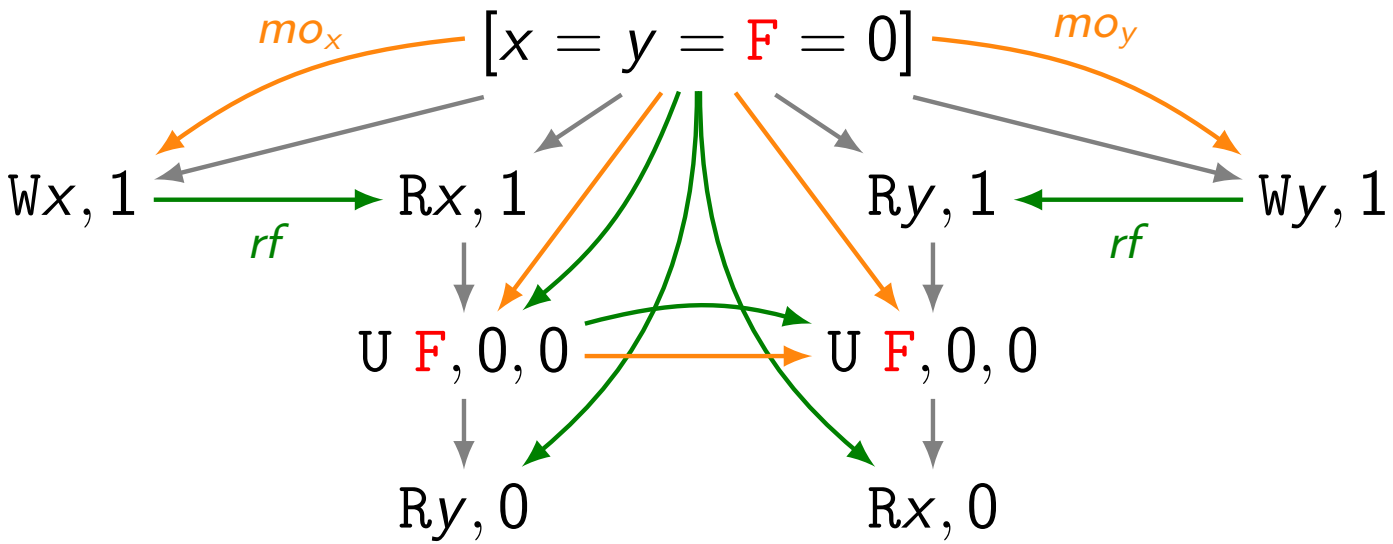

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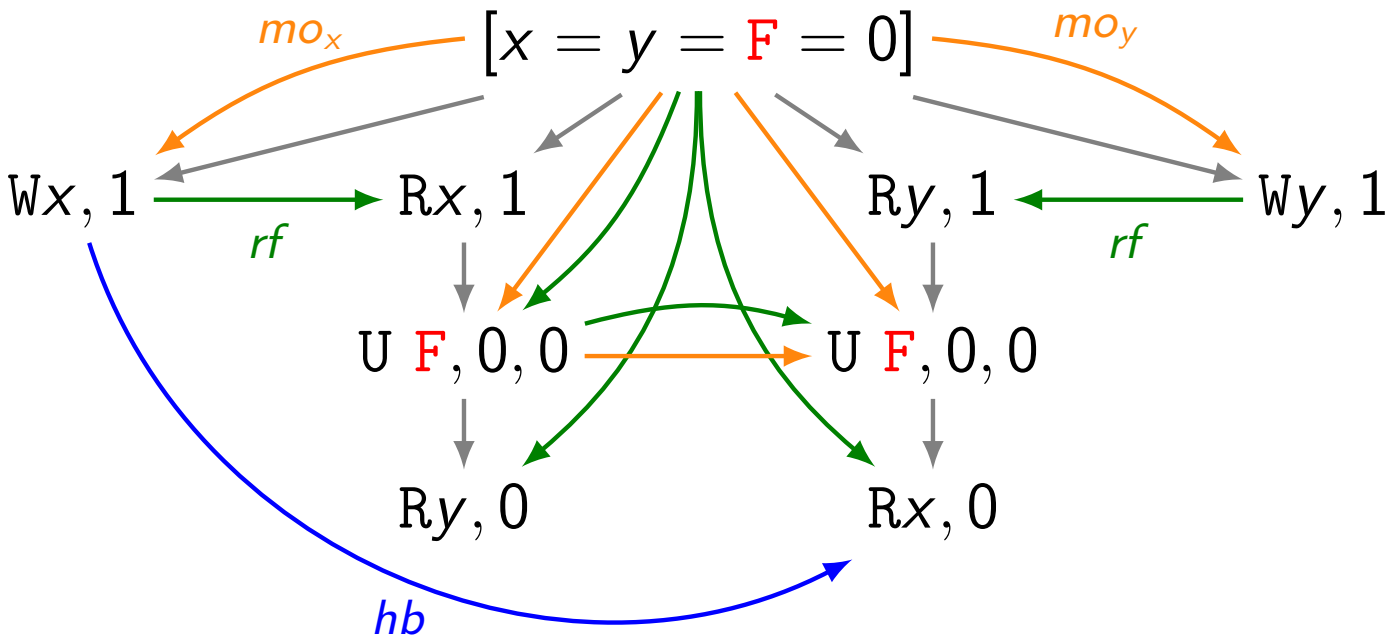


Inconsistent: $\mathtt{R}x, 0$ reads an overwritten value

Compilation schemes are not affected

x86-TSO

- SC-fence $\hookrightarrow$ `mfence`
- Atomic update $\hookrightarrow$ `lock xchg`
- `mfence` and `lock xchg` of an unused value have the same operational effect.

Power

- `sync` events are equivalent to a acquire/release atomic updates from an otherwise-unused location.

Reductions to SC

Theorem (basic reduction)

If a program includes a fence between every two racy accesses to different shared variables, then it has only SC behaviors.

- Under x86-TSO, it suffices to have a fence between racy writes and subsequent racy reads.

$x := e;$
`fence();`
$r := y$

Theorem (advanced reduction, simplified version)

For client-server programs, it suffices to place fences as under x86-TSO.

In the paper: application to an RCU implementation.

3. An Operational Presentation

- Easier to understand by simulating step-by-step progress
- Foundation for traditional verification techniques

Example: the SRA machine (first attempt)

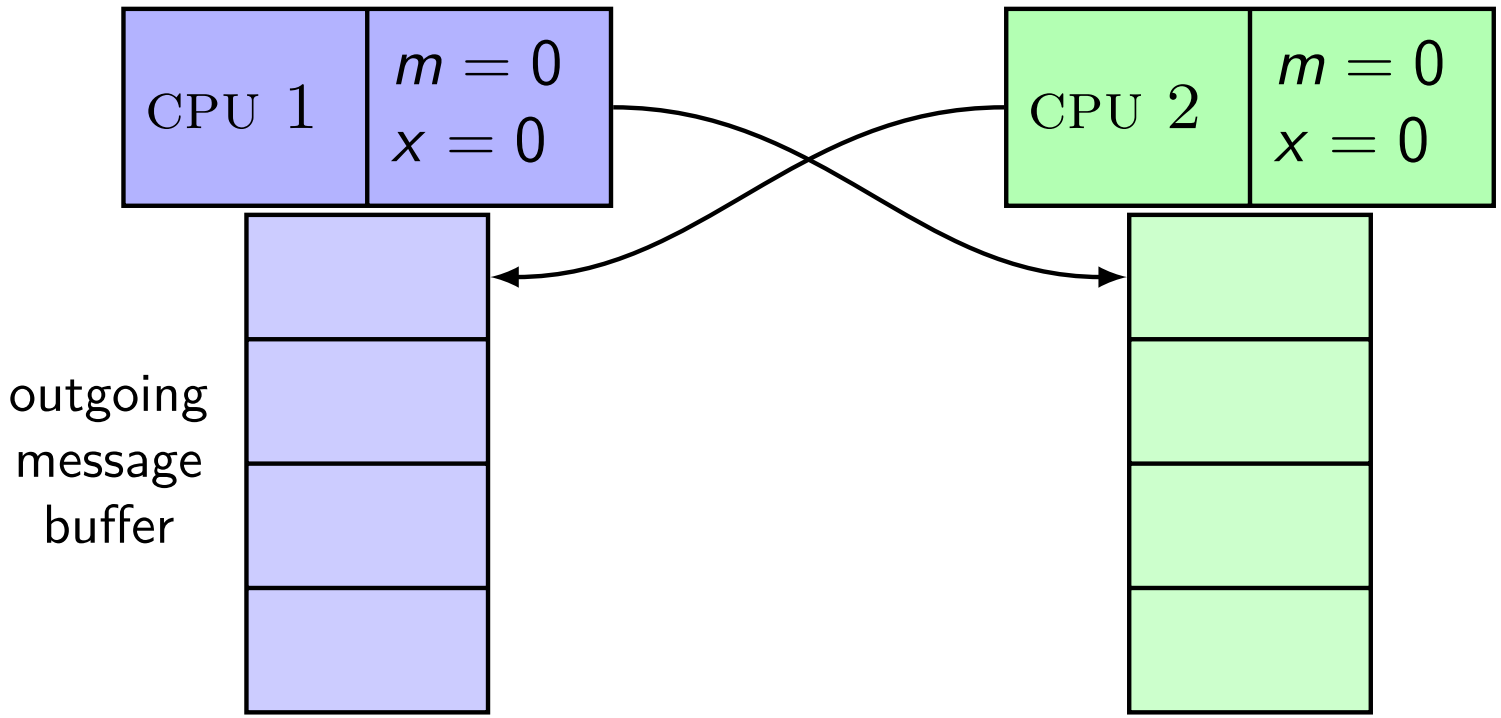
Message passing

$m = x = 0$

- $m := 42$;
  $x := 1$

$\parallel$

- `while` $x = 0$
  `skip`;
  `print` m



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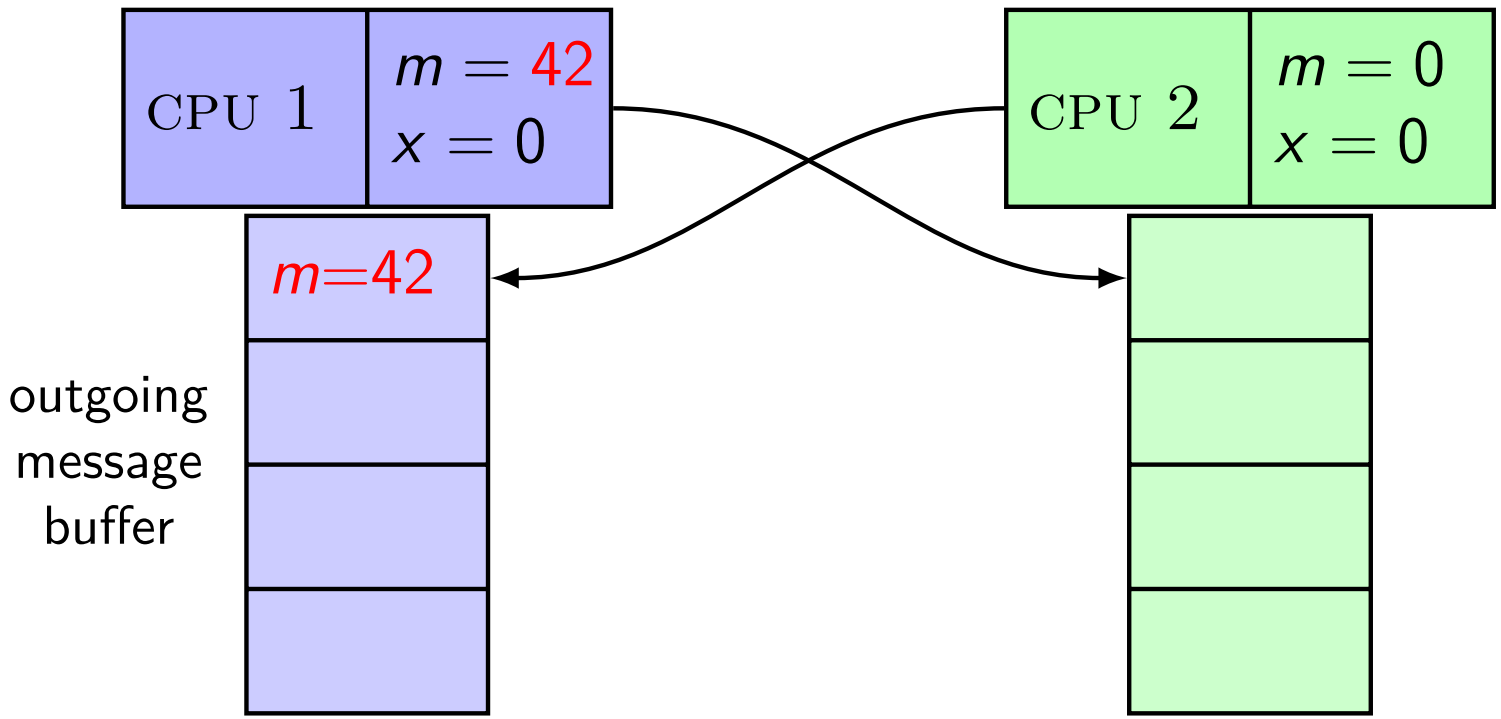

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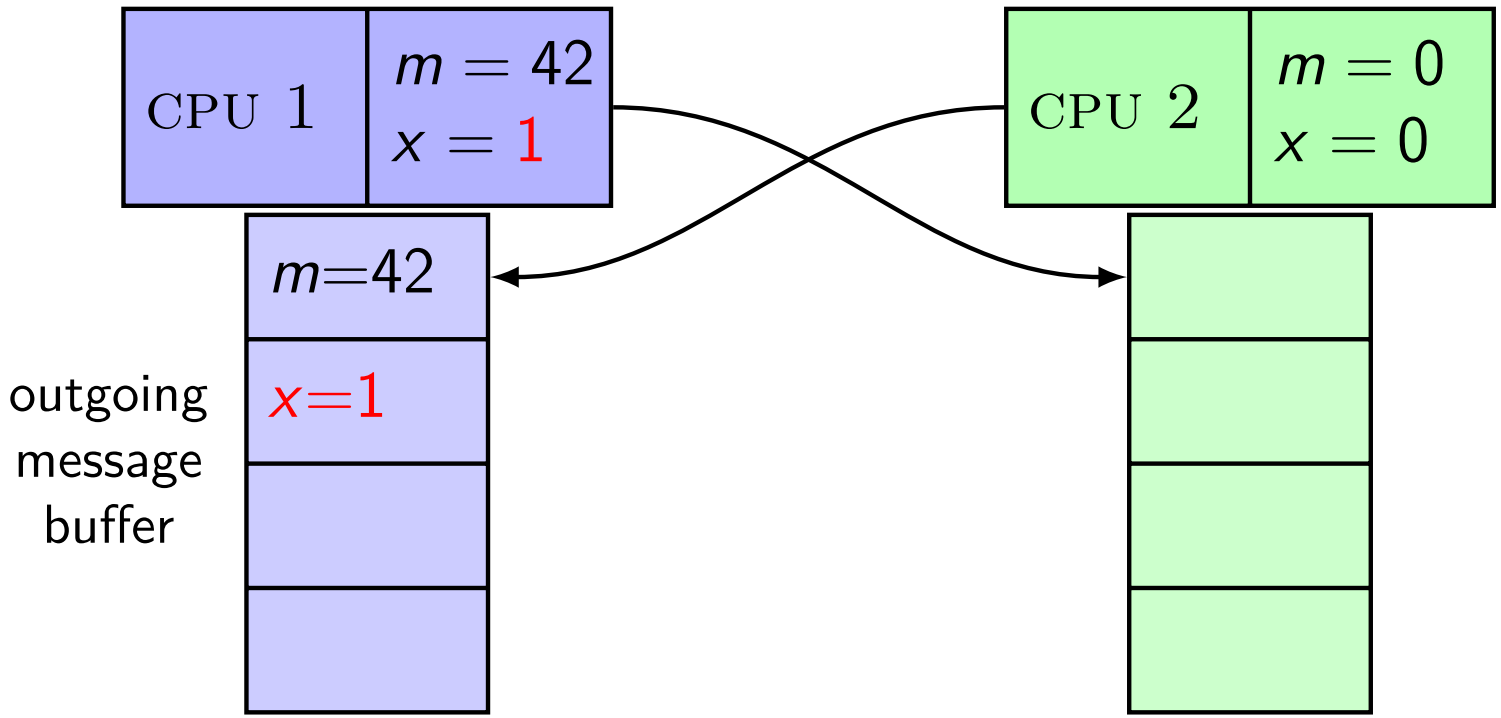

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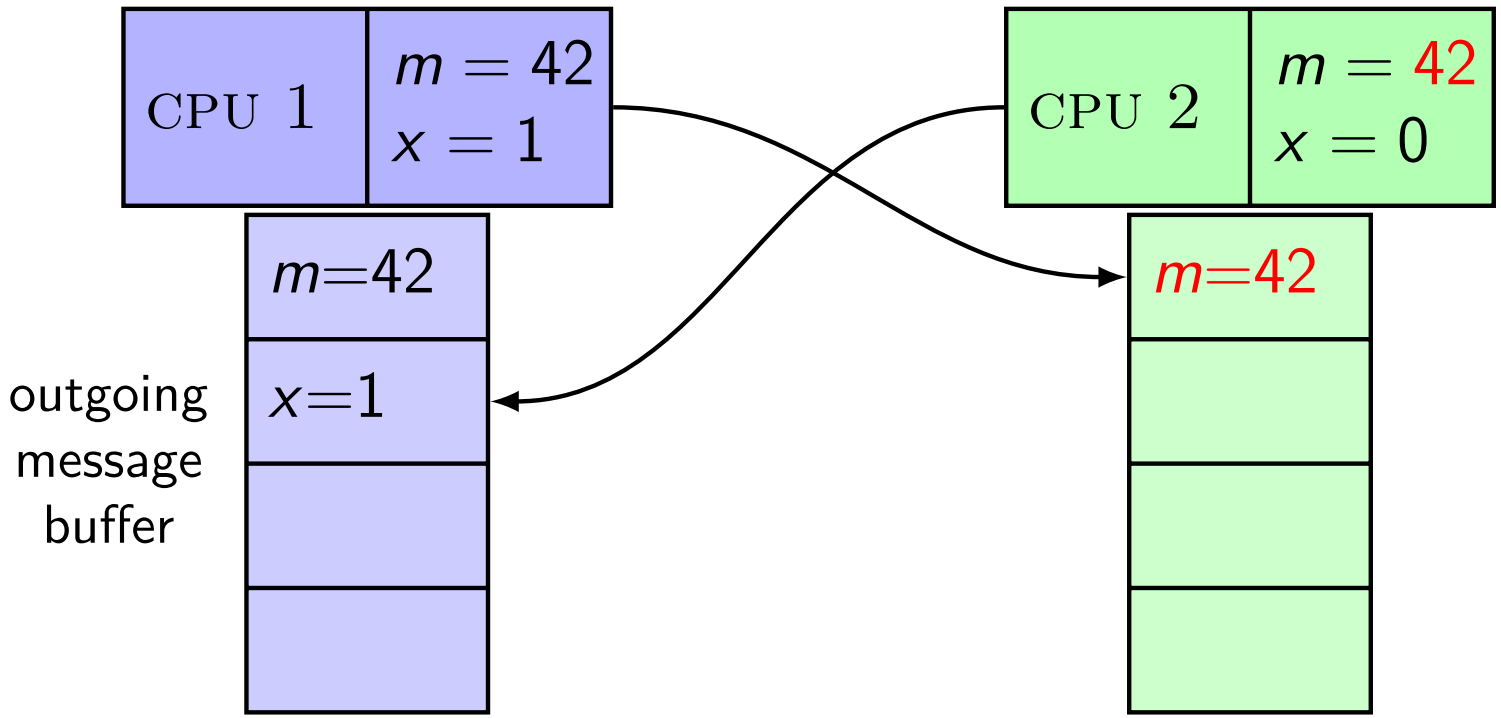

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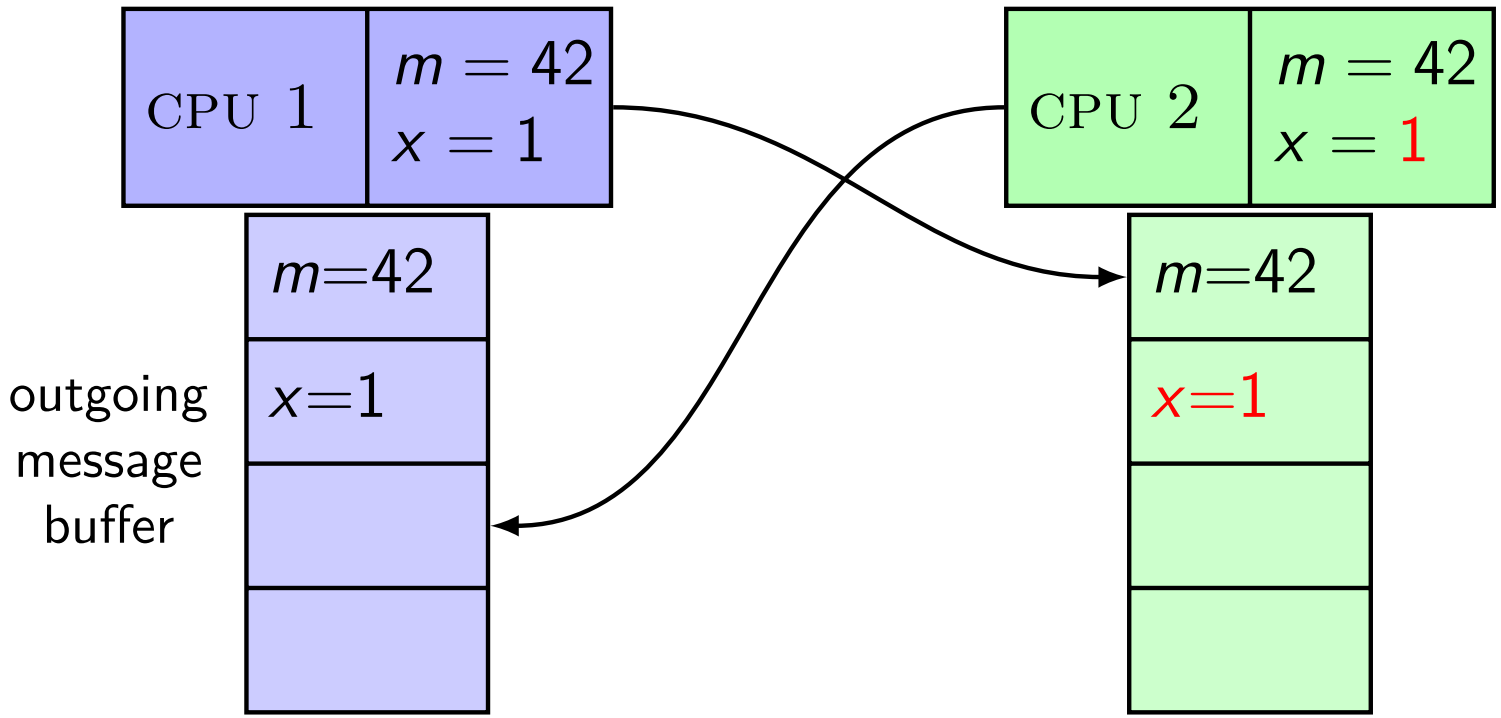

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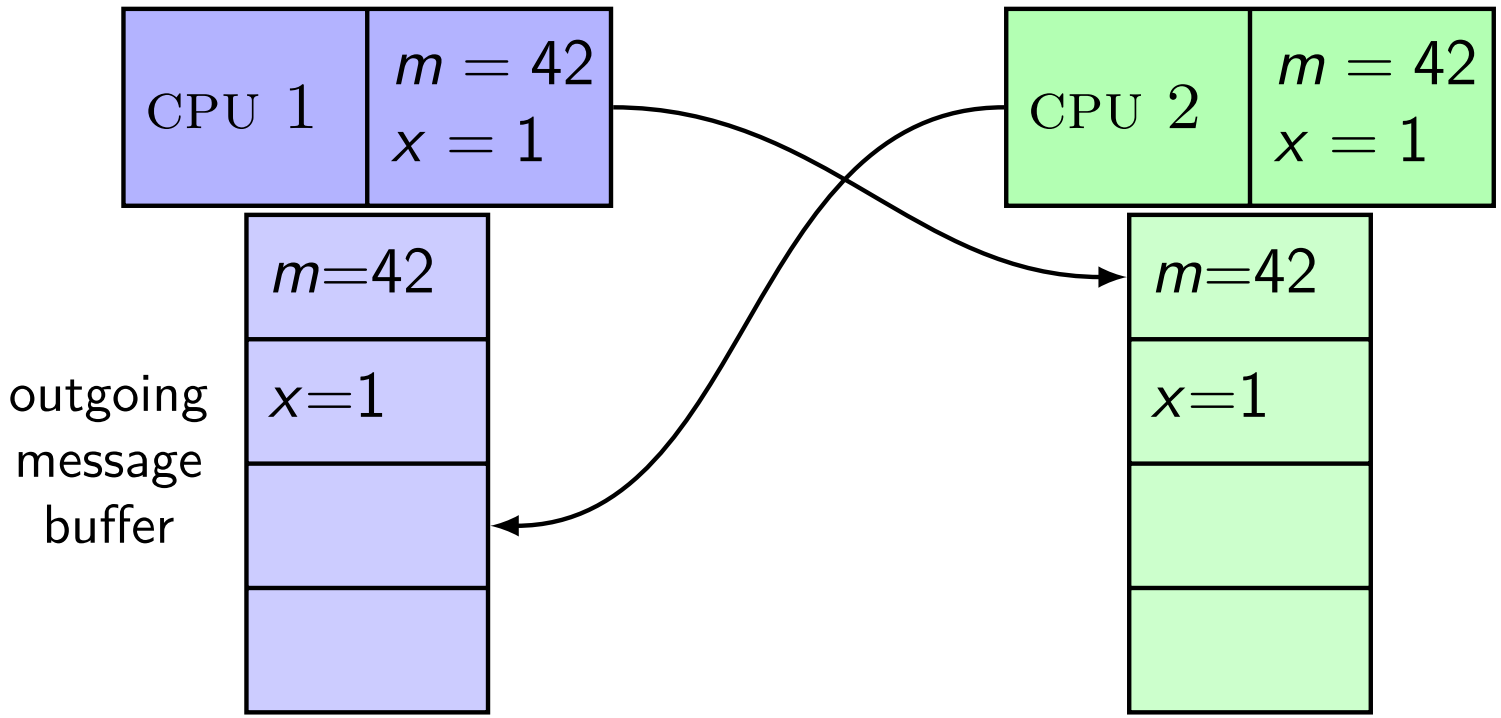

Timestamps

$$
\begin{array}{l}
x := 6; \\
\texttt{if } x = 7 \\
\quad \texttt{print } \text{`}go\text{'}
\end{array}
\quad \Big\| \quad
\begin{array}{l}
x := 7; \\
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$$

'*go*' should be printed at most once

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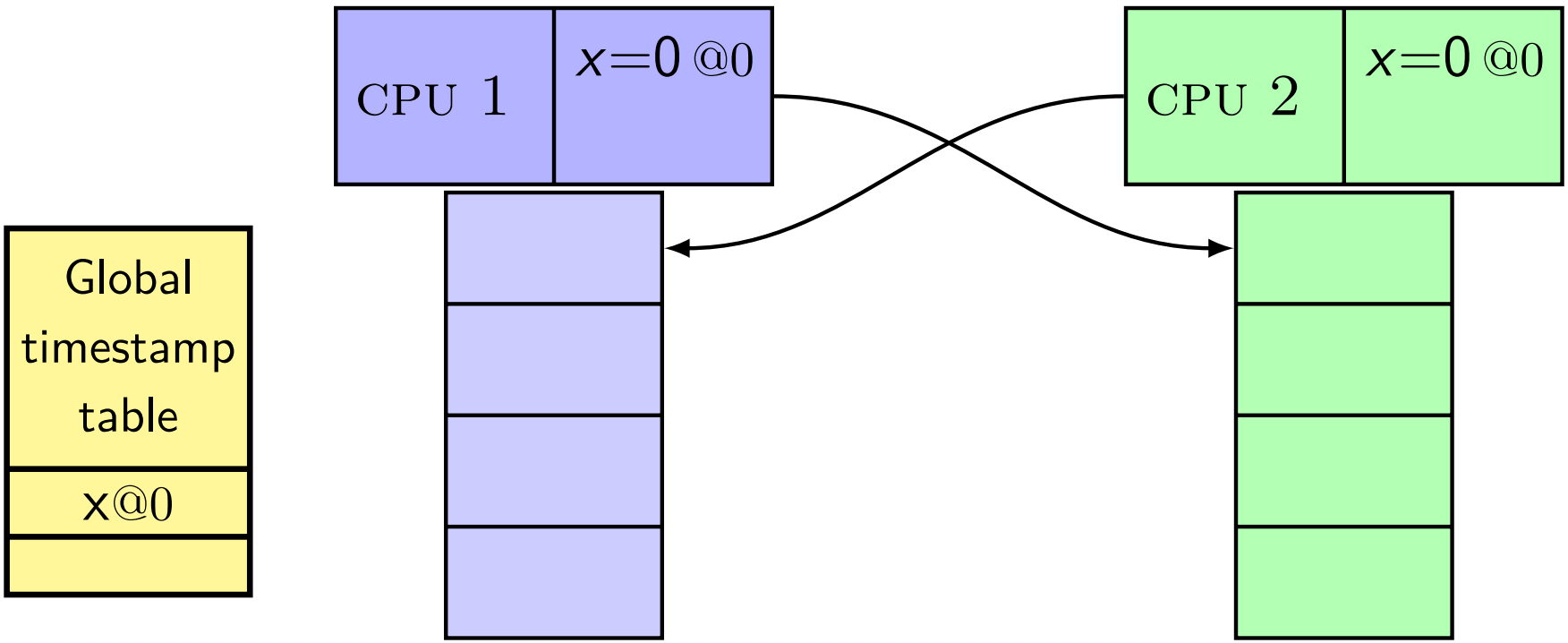

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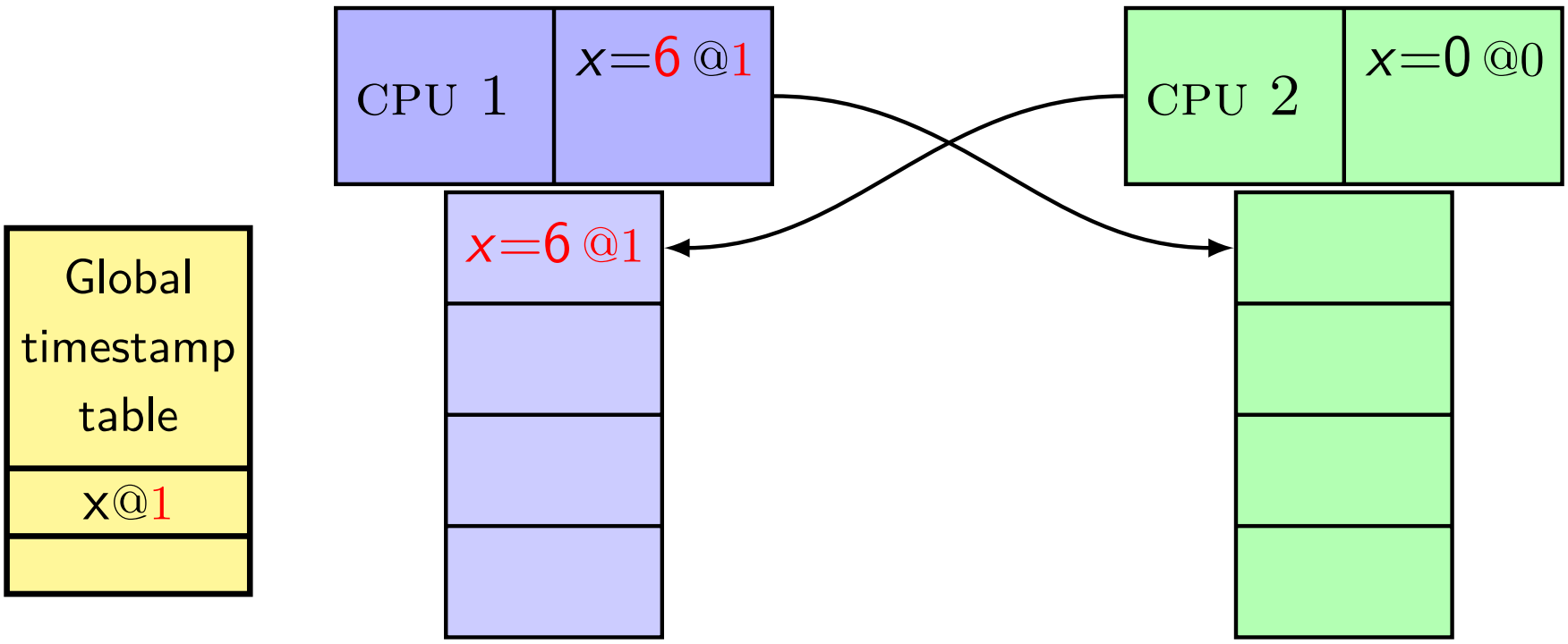

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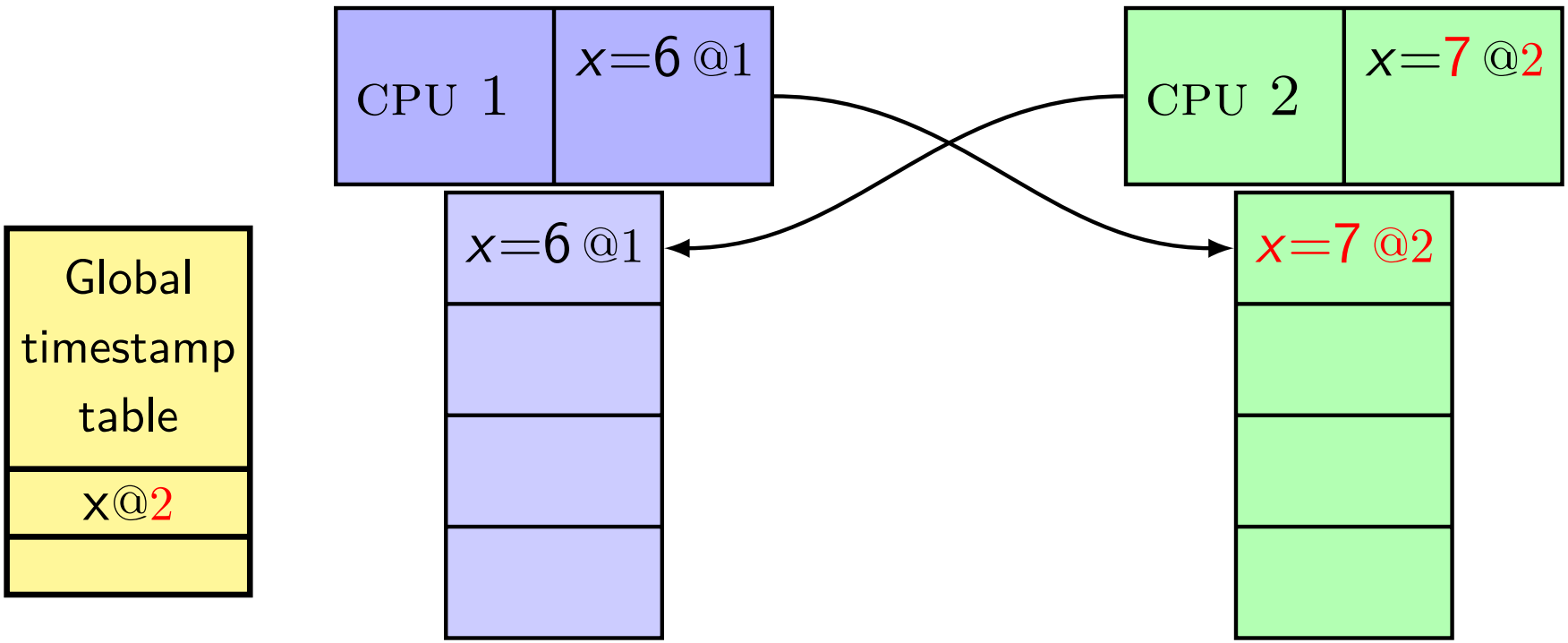

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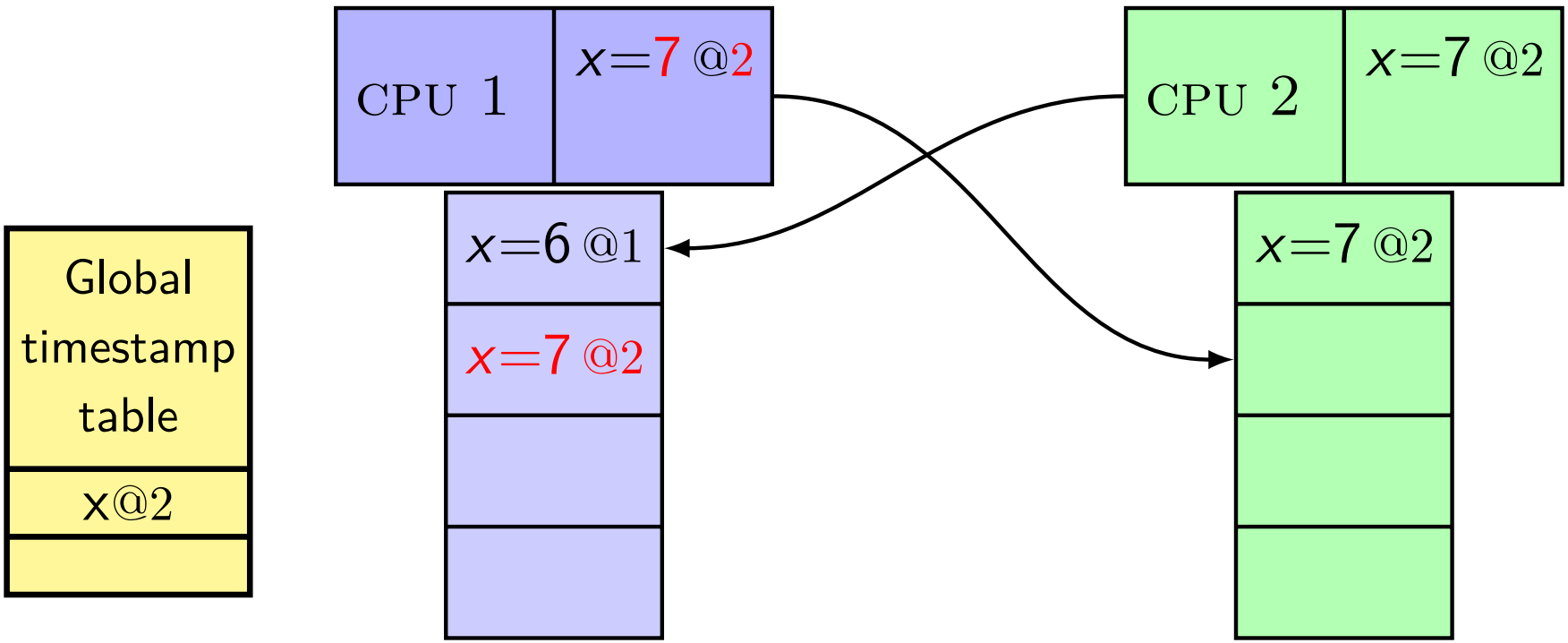

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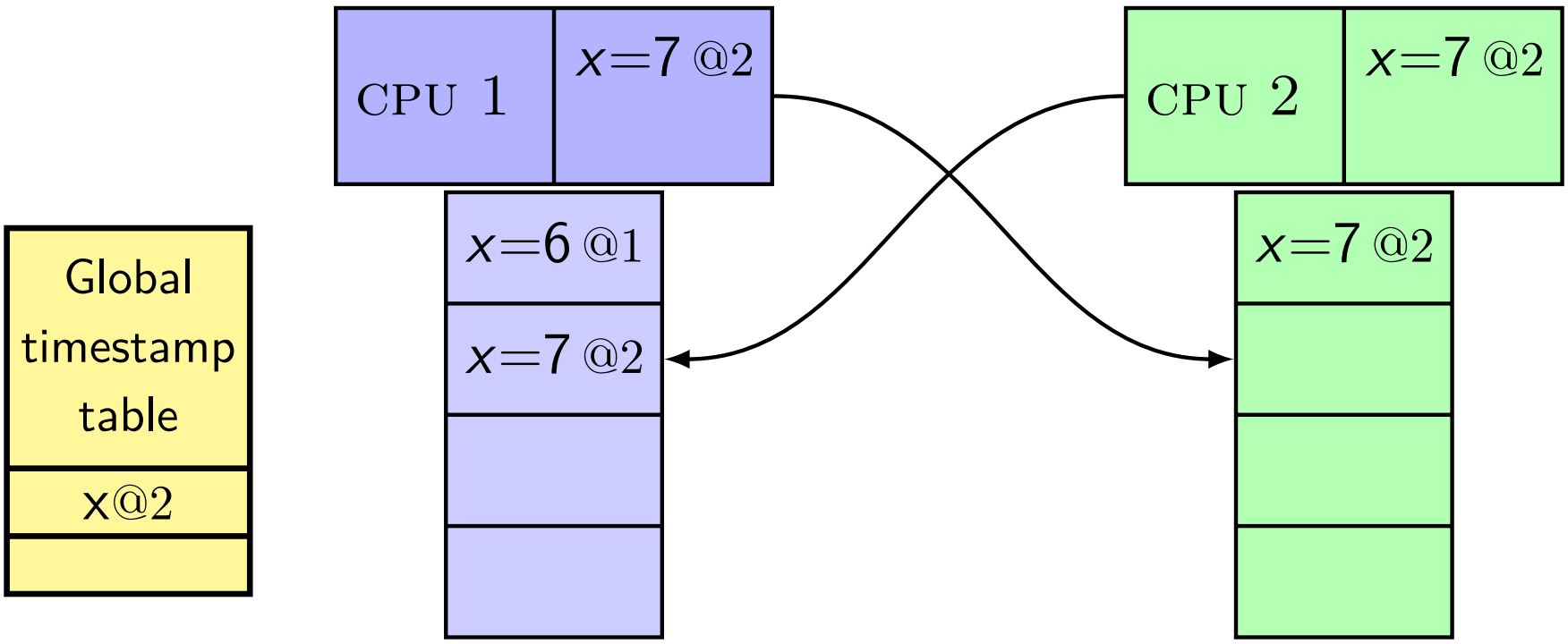

Timestamps

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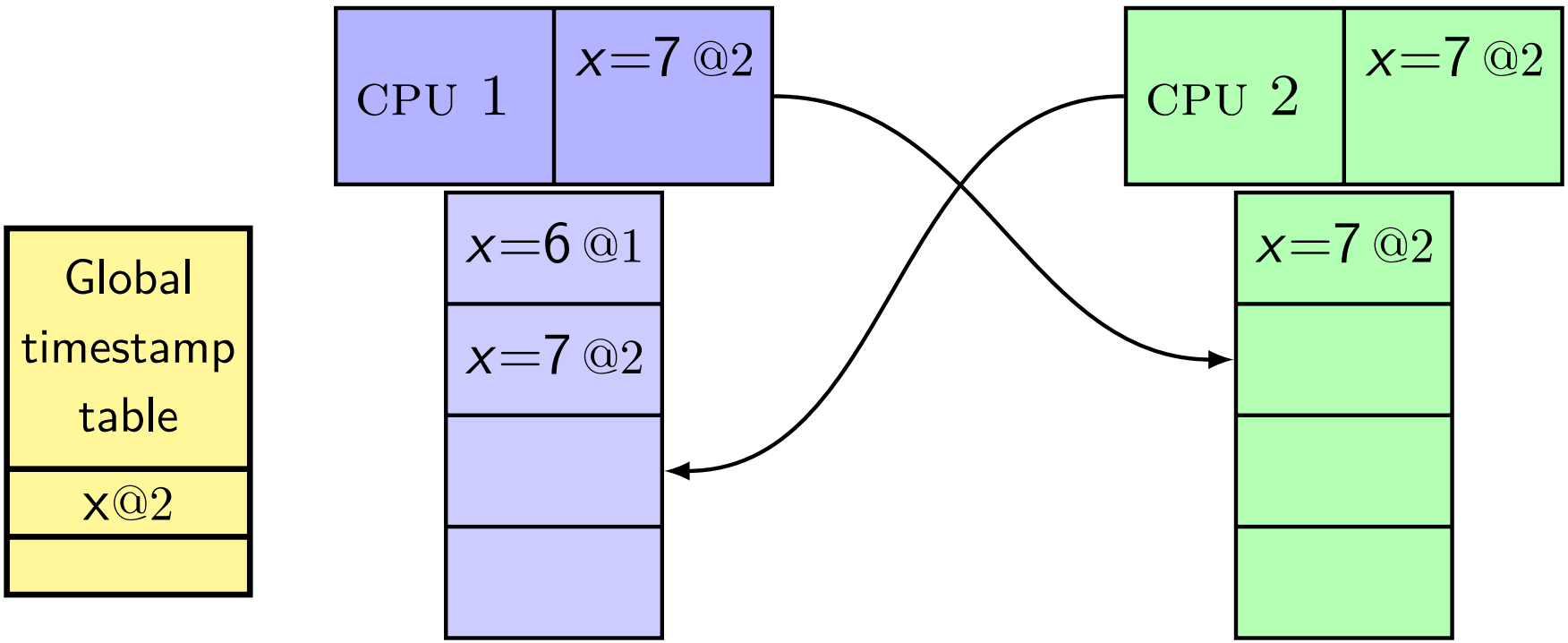

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- We propose a strengthening of this memory model that:
  - forbids weak behaviors, unobservable in any implementation
  - has simple fence semantics, with SC-reduction theorems
  - admits intuitive operational semantics
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